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08/20/02

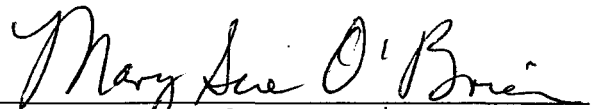
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FROM: Logistics and Technical Information Division  
SUBJECT: Notification of Clearance - CL#02-2164

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# **Single-Event Upset in Power-PC Processors**

**G. M. Swift, A. H. Johnston, and F. Irom**

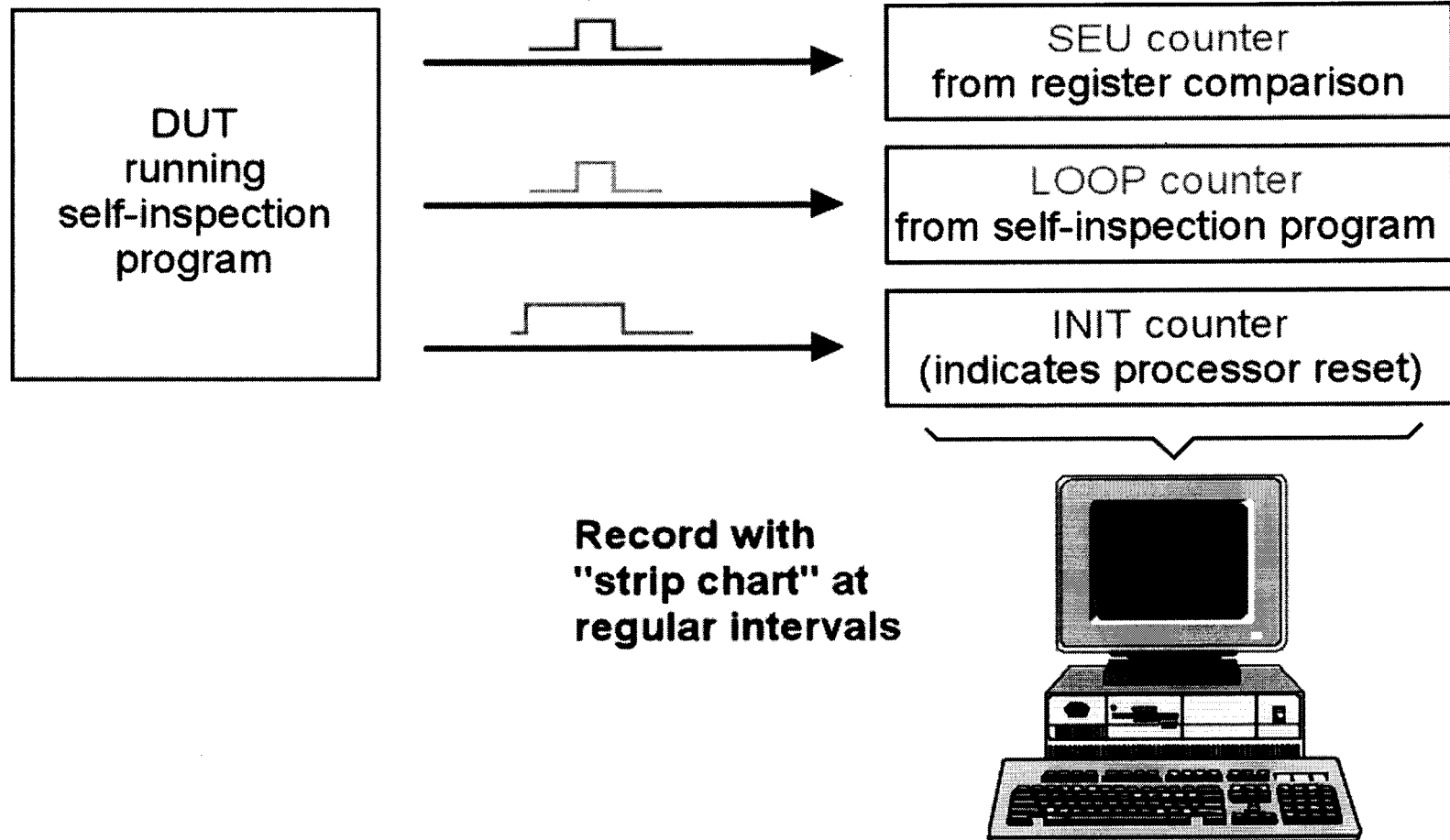
Jet Propulsion Laboratory  
California Institute of Technology  
Pasadena, CA 91109 USA

The research in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA), under the NASA Electronics Parts and Packaging Program, Code AE.

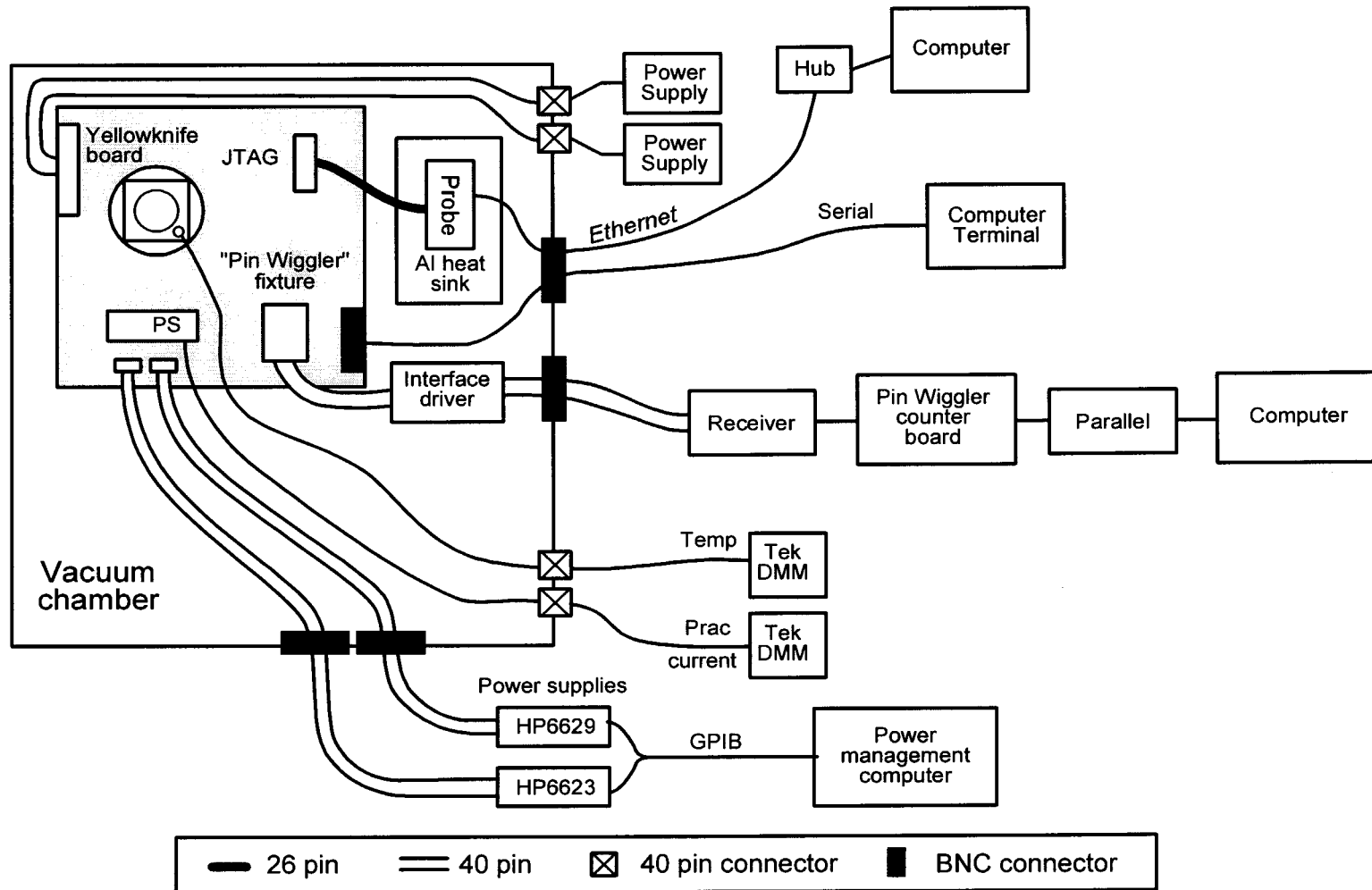
# Outline

- **Background**
  - Processor Testing
  - PowerPC family
- **Proton Tests**
- **Heavy Ion Tests**
- **Discussion**
  - Hangs and Crashes
  - Effects of Scaling
- **Conclusions**

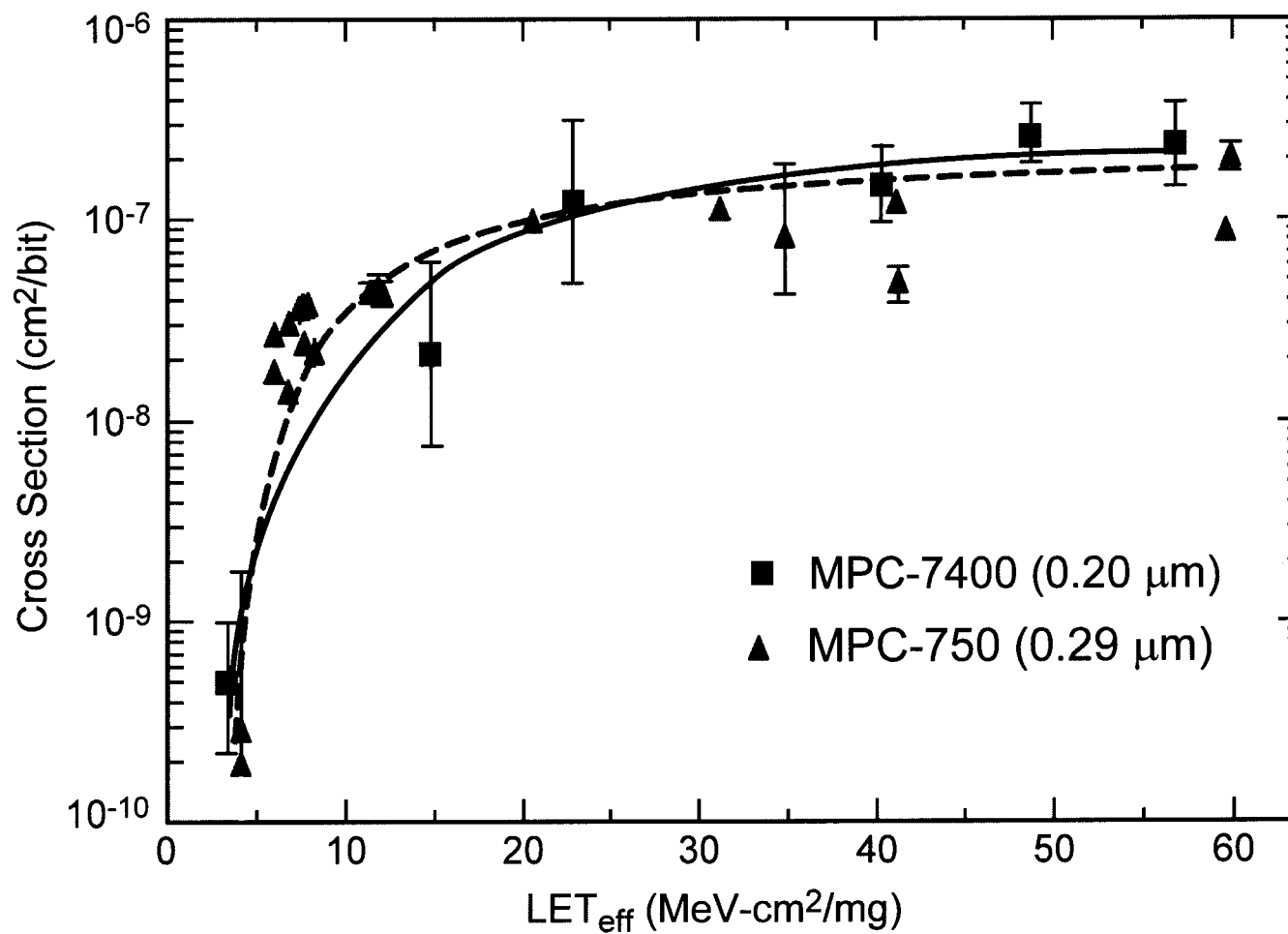
# Overview of “Pin Wiggler” Method



# Test Approach Using “Yellowknife” Development Board

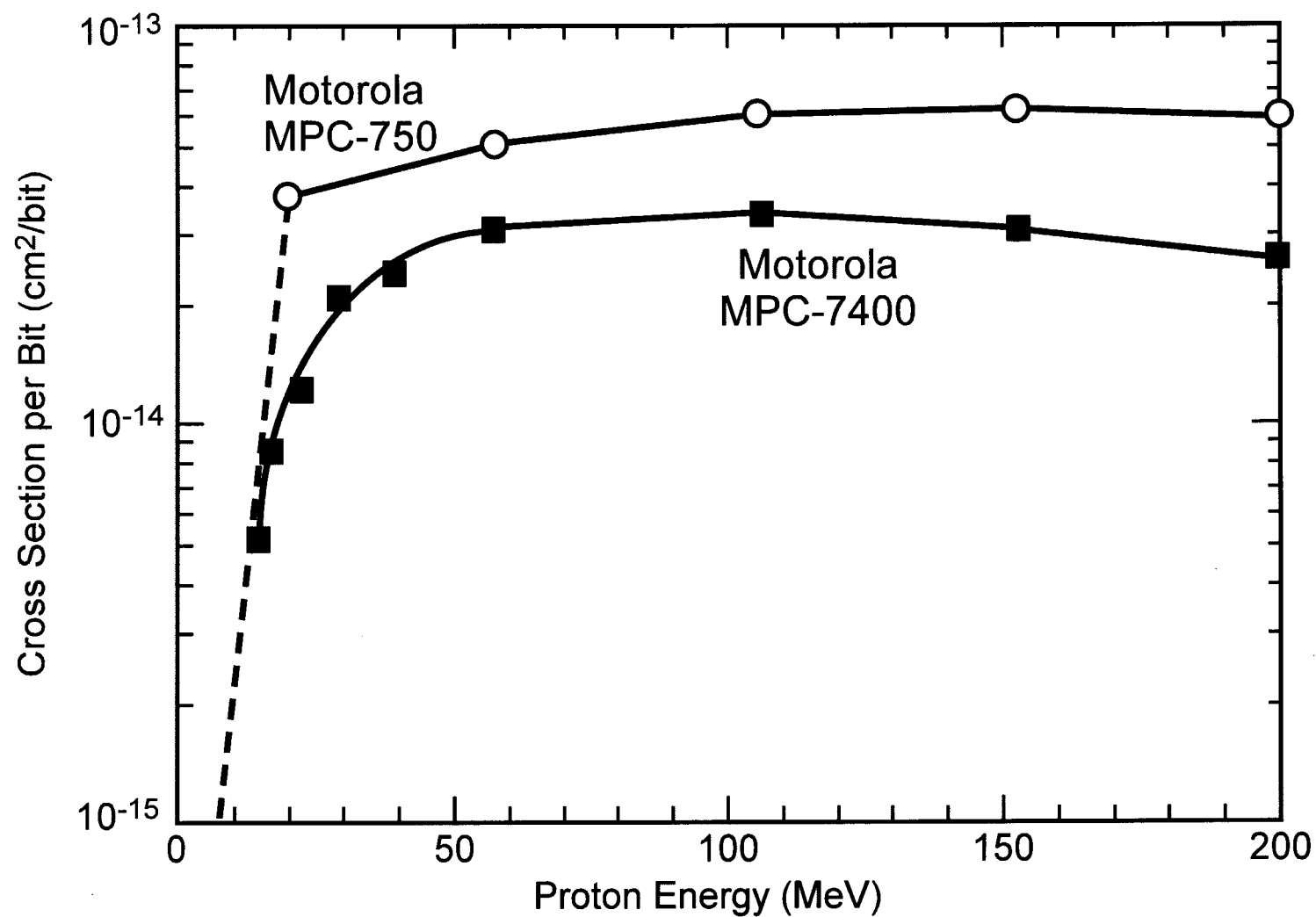


# Proton Upsets of PowerPC Cache





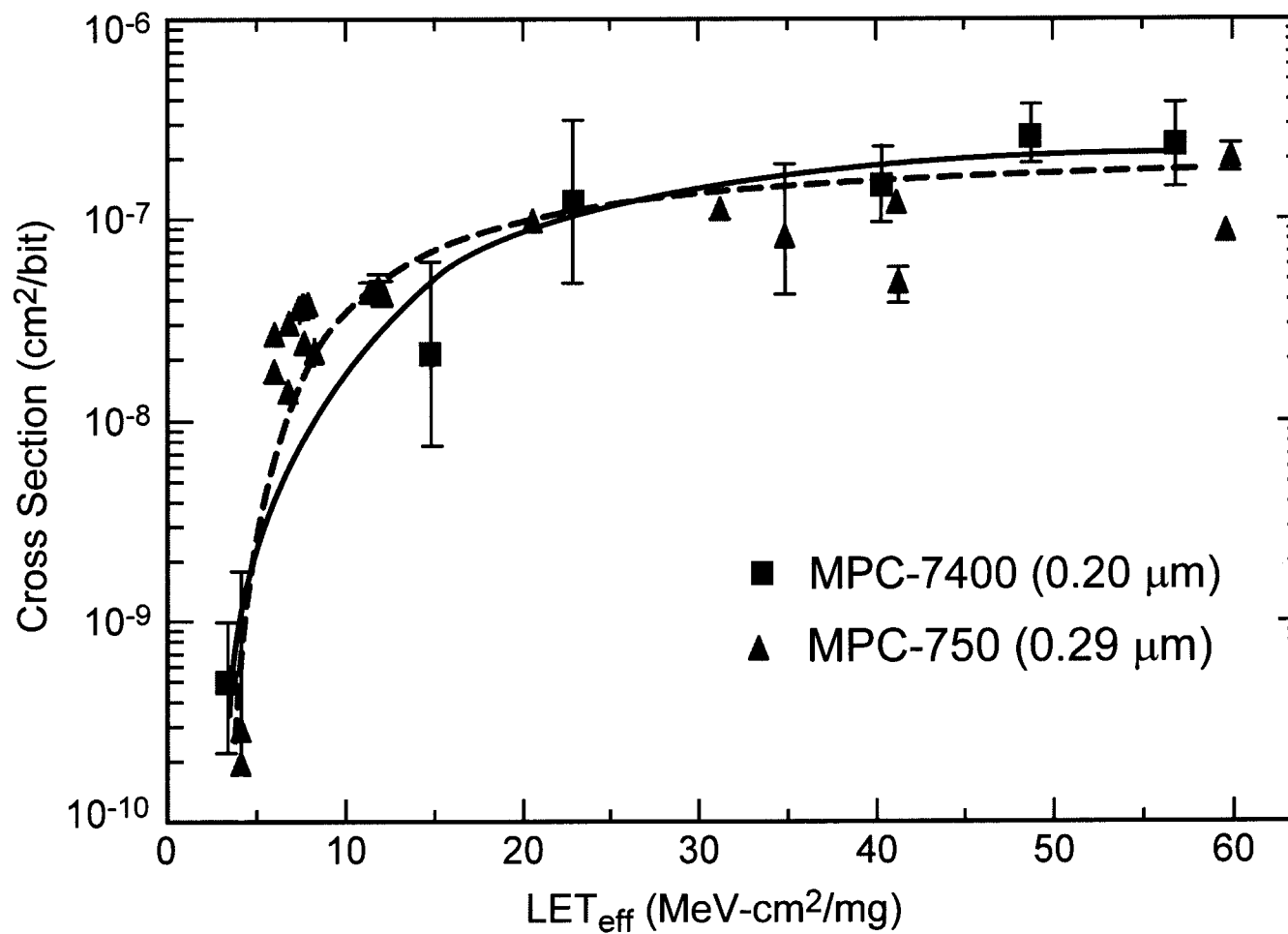
# Proton Upset Results for FPRs



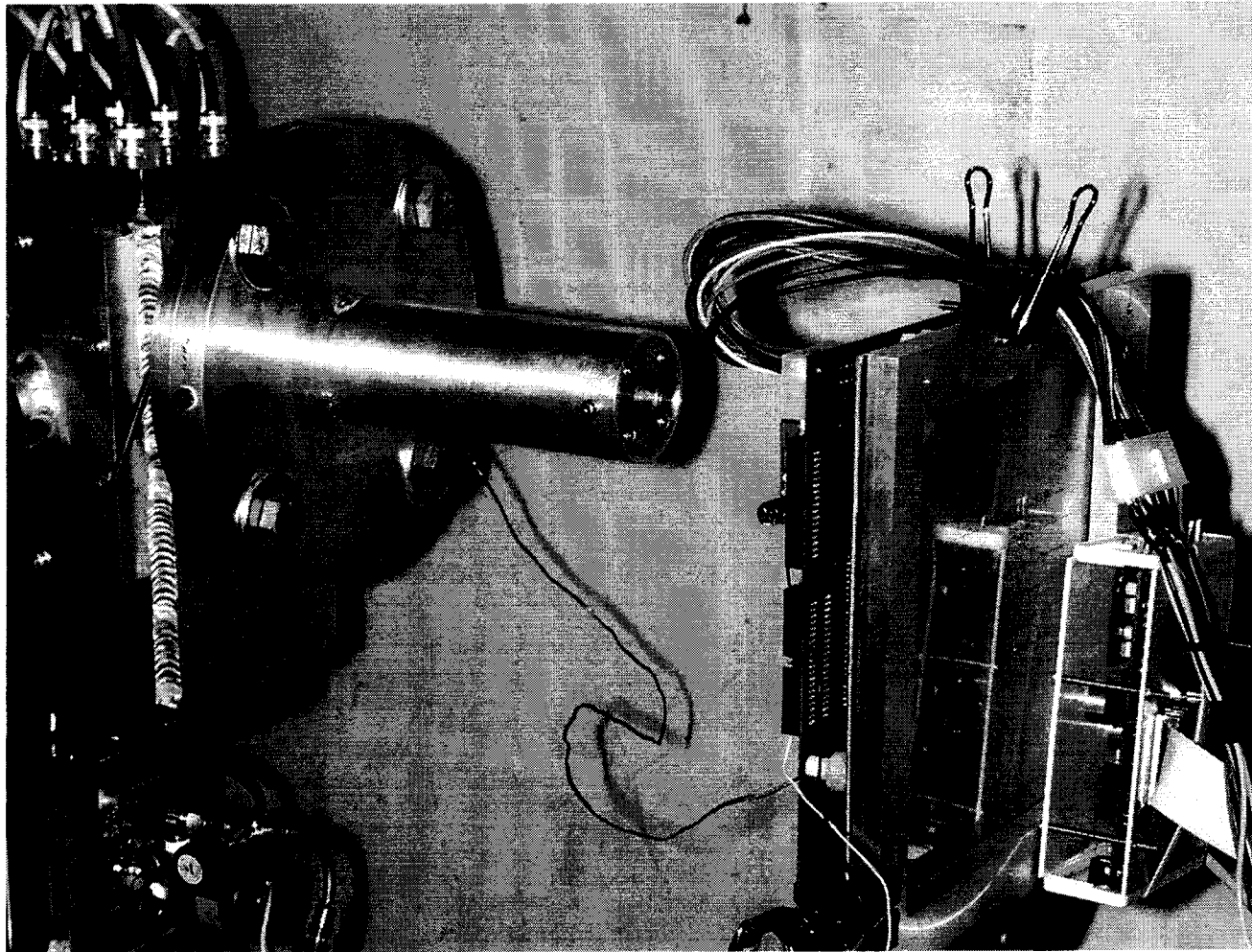
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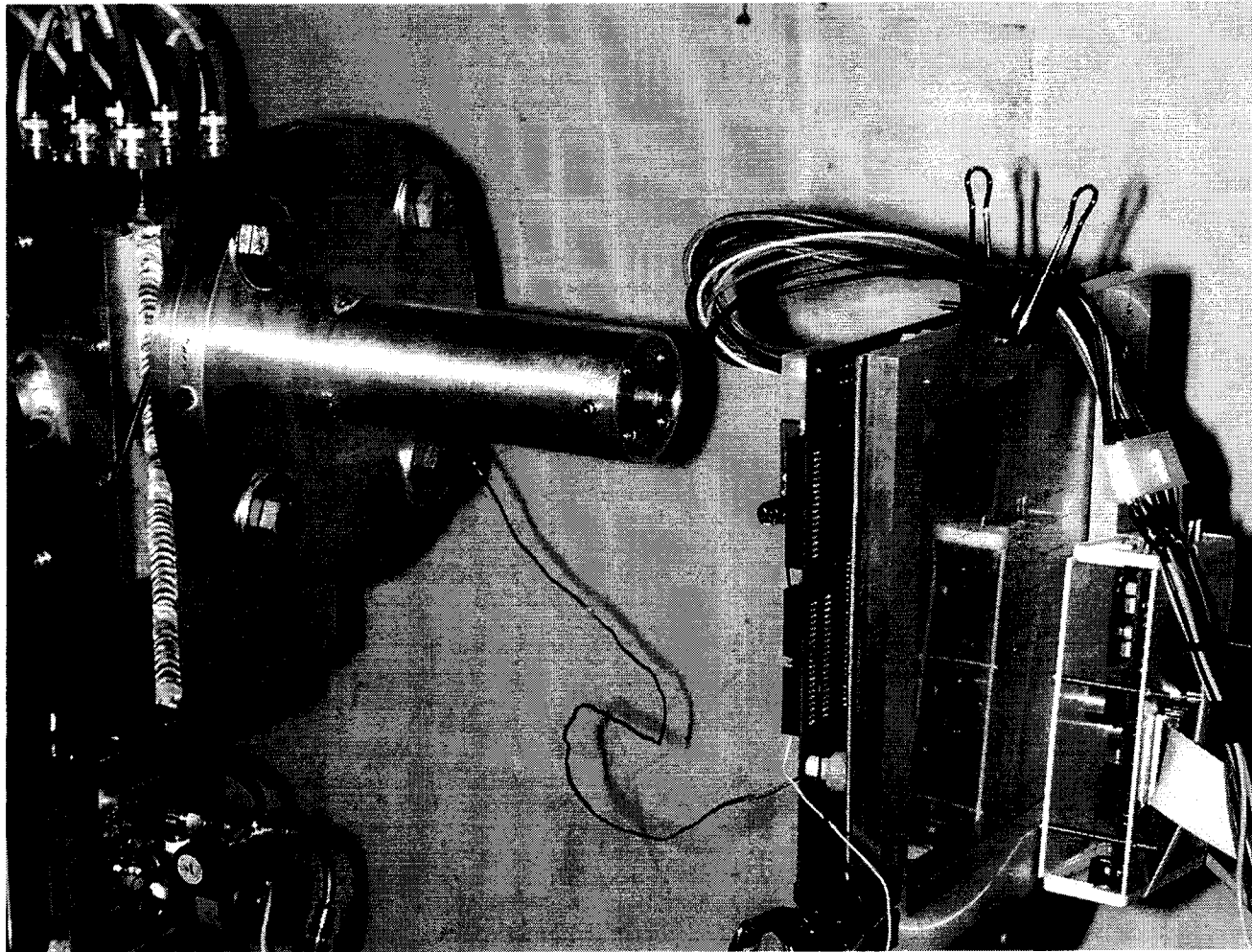
# Proton Upsets of PowerPC Cache



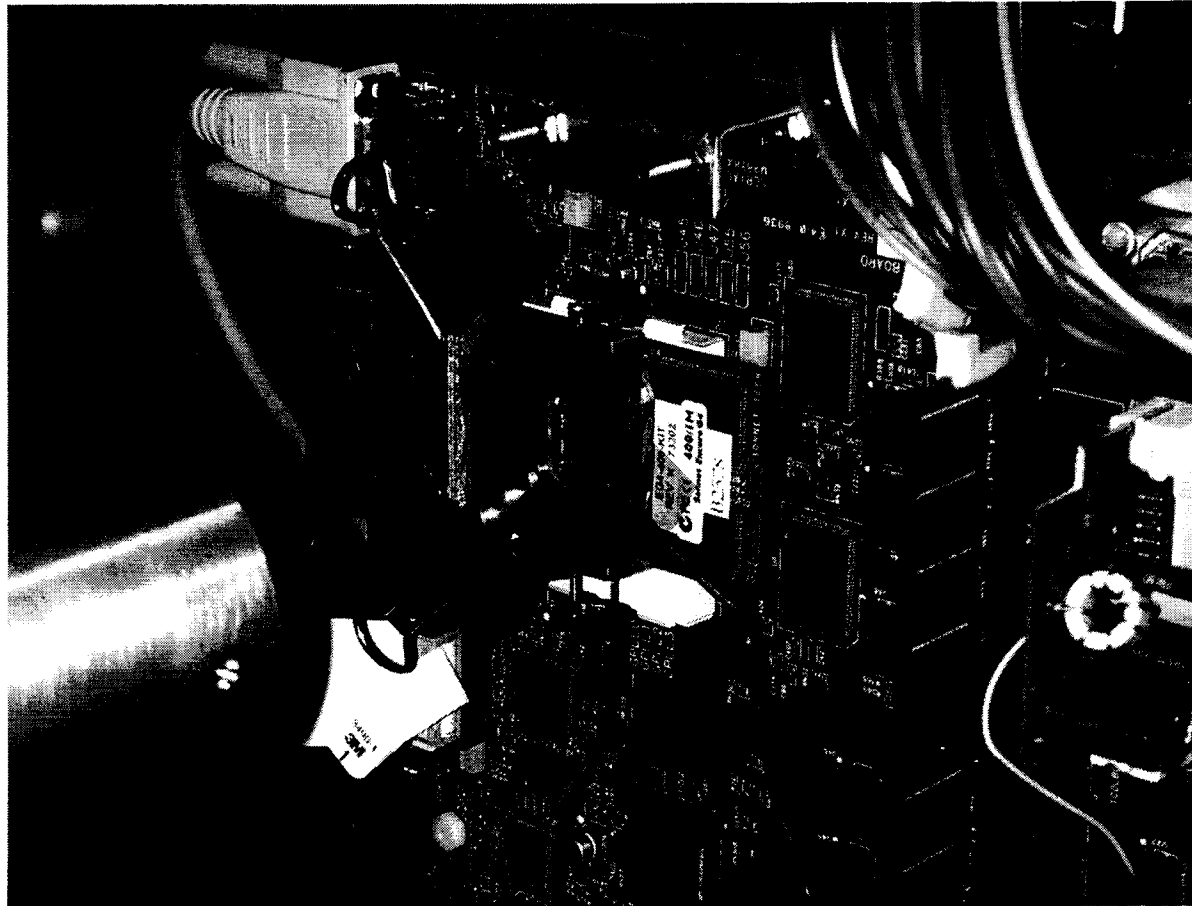
# TAM In-Air Irradiation Facility



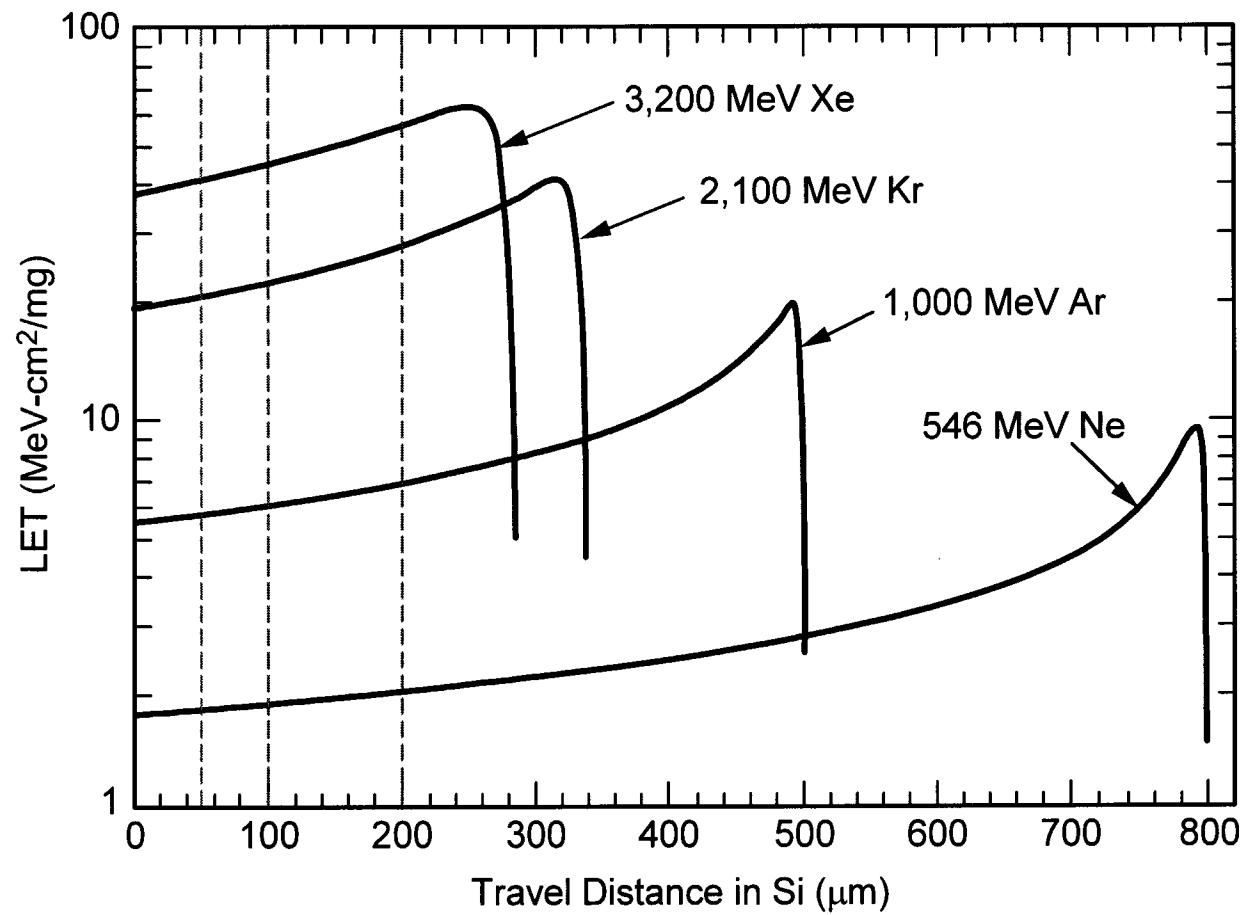
# TAM In-Air Irradiation Facility



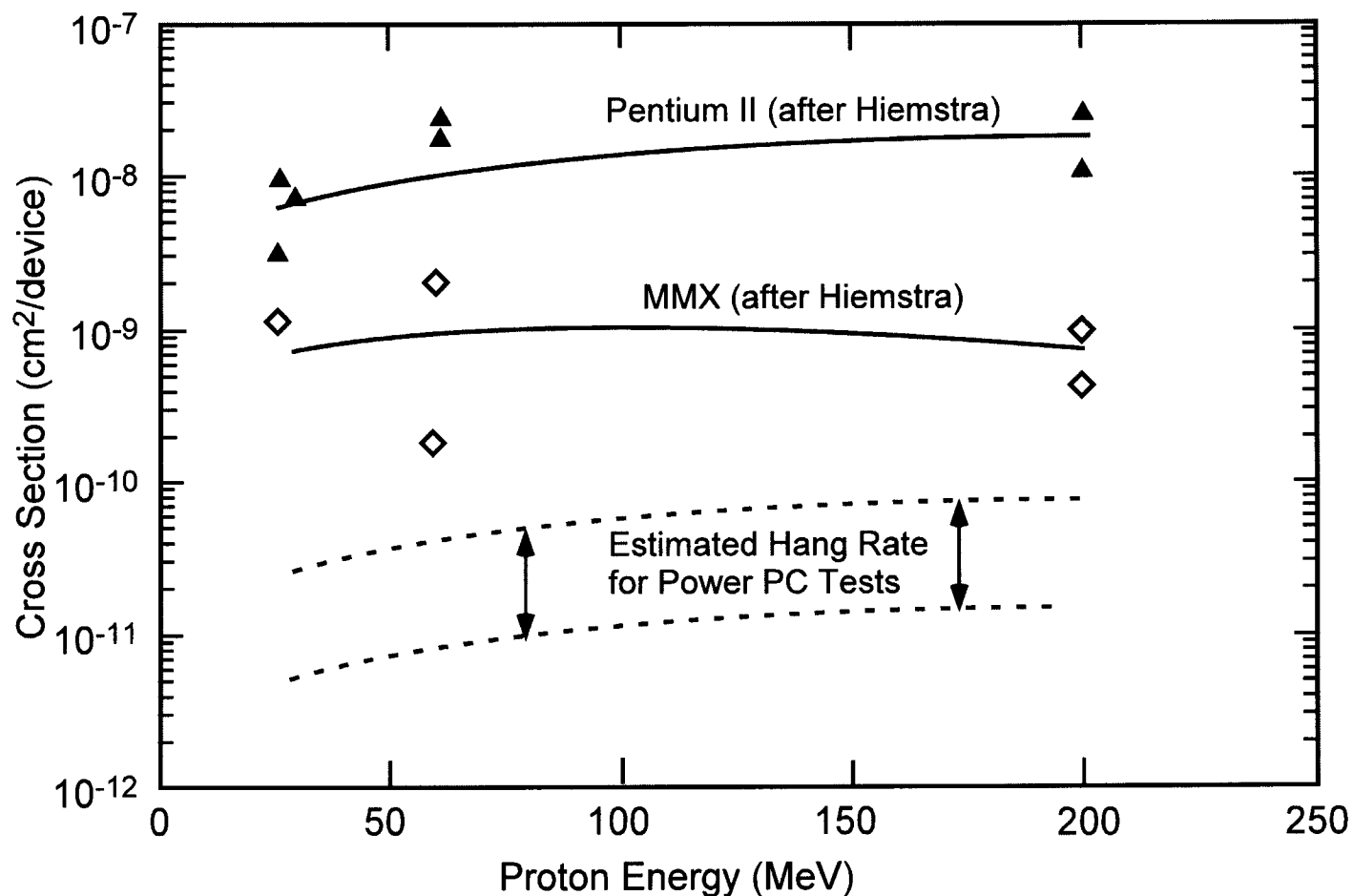
# Dealing with Thermal Problems



# Heavy Ions Used

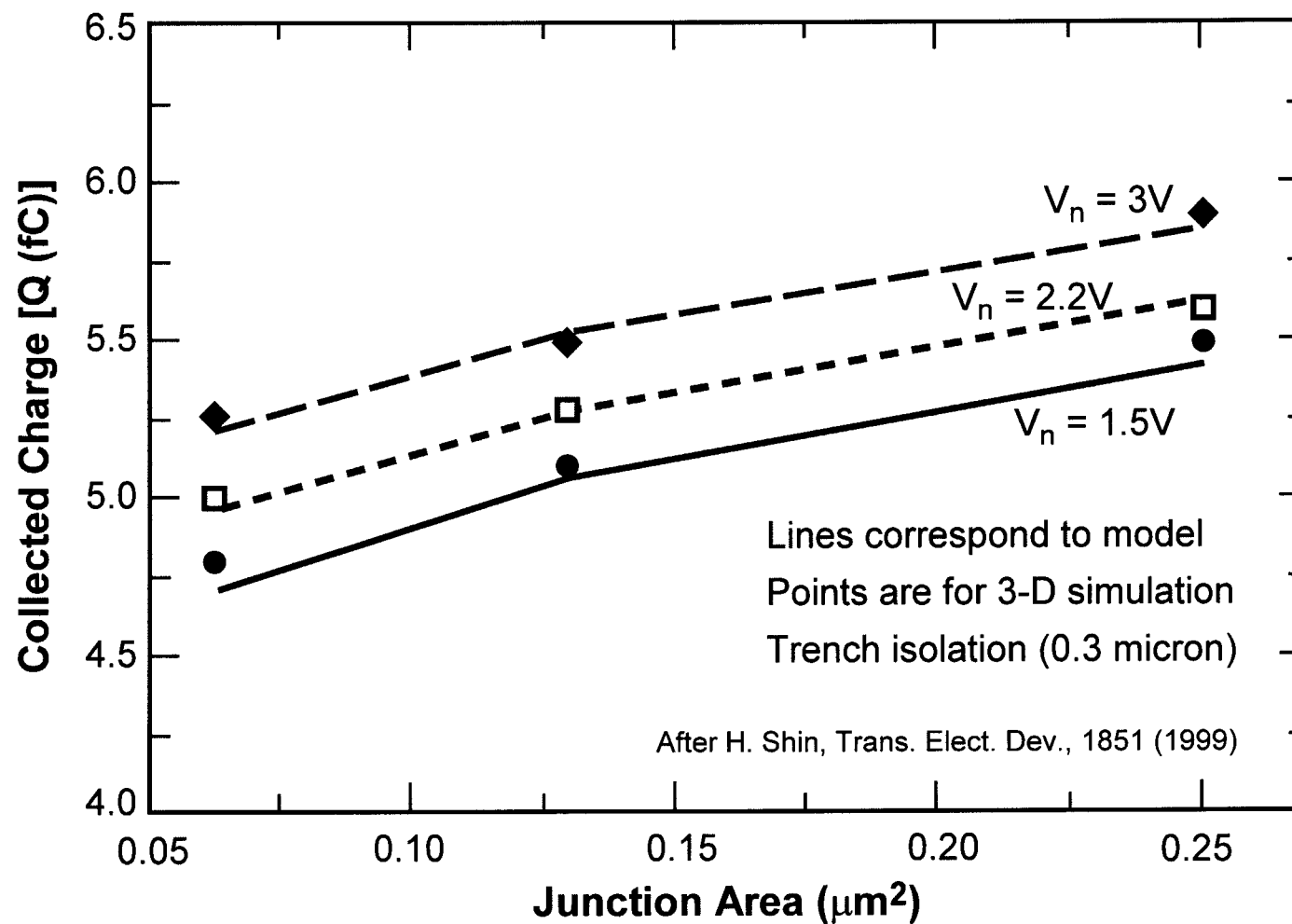


# Hang Comparison: PowerPCs and Pentiums





# Scaling: Alpha Simulation Results



# Conclusion

- **Processor Test Techniques**
  - Hand coded assembly test programs
  - Simple or no operating system
- **Upset Results**
  - Cache and register upsets dominate at present
  - Hangs and crashes expected to increase
- **Scaling Results**
  - Cross sections lower with smaller feature sizes
  - Consistent with charge collection simulations

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